IN THE CLAIMS

Please amend claims as follows:

1. (Amended) An apparatus comprising:

an internal test bus (ITB);

a plurality of deskew clusters coupled to the ITB, wherein the plurality of deskew clusters each include a deskew controller;

an integrated test controller (ITC) coupled to the ITB; and

a debug unit coupled to the ITC;

wherein the ITC generates a single global control signal and each of the deskew controllers generates a first local [command] control signal.

2. (Amended) The apparatus of claim 1, wherein each of the plurality of deskew clusters further comprise a plurality of deskew buffers and a regional clock driver (RCD).

3. (Amended) The apparatus of claim 1, wherein each of the deskew controllers further generates [comprising] a second local command signal, wherein the single global control signal and one of the first local command signal, the second local command signal, and both the first local command signal and the second local command signal provide a distributed test control scheme for integrated circuits including debug and testability operations.

Please add the following claims:

--16. A system comprising:

at least one processor;

a global bus coupled to the at least one processor;

a memory coupled to the global bus;

an internal test bus (ITB) located within the at least one processor;

a plurality of deskew clusters coupled to the ITB, wherein the plurality of deskew clusters each include a deskew controller;

an integrated test controller (ITC) coupled to the ITB; and

a debug unit coupled to the ITC;

wherein the ITC generates a single global control signal and each of the deskew controllers generates a first local control signal.--

--17. The system of claim 16, wherein each of the plurality of deskew clusters further comprise a plurality of deskew buffers and a regional clock driver (RCD).--

--18. (New) The system of claim 16, wherein each of the deskew controllers further generates a second local command signal, wherein the single global control signal and one of the first local command signal, the second local command signal, and both the first local command signal and the second local command signal provide a distributed test control scheme for integrated circuits including debug and testability operations.--

--19. The system of claim 16, wherein the first local command signal is a snapshot instruction and the second local command signal is a shift instruction.--

--20. The system of claim 19, wherein a snapshot instruction can be issued at a first time period and a shift instruction can be issued at a second time period, and